THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HUMBERTO F. CASAL,
HEHCHING H. LI,
and DAVID MING-WHEI WU

Appeal No. 1998-1365
Application No. 08/663,969

ON BRIEF

Before THOMAS, JERRY SMITH, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 27, 28, 31-33, 35-37, 40-42, and 44.[1] We affirm.

[1]A rejection not referred to in an examiner's answer is assumed to have been withdrawn. Ex parte Emm, 118 USPQ 180,

(continued...)

BACKGROUND

A computer's clock rate is a prime determinant of its overall processing speed. A clock typically operates at a frequency of 50-150 MHZ. To achieve higher performance, a microprocessor may generate an on-chip clock signal by multiplying the frequency of an off-chip clock source. Accordingly, a 50-MHZ off-chip source can be used to generate on-chip clocking of 200 MHZ. Unfortunately, techniques to check on-chip clocking during manufacturing are complex and time consuming.

The invention at issue in this appeal is a test circuit for determining whether an on-chip clock signal is a correct multiple of a reference clock signal and whether the two signals are in-phase. Specifically, the test circuit, a

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[1](...continued)
181 (Bd. Pat. App. & Int. 1958) (citing Ex parte Charch, 102 USPQ 363, 364 (Bd. Pat. App. & Int. 1954) and Ex parte Hill, 93 USPQ 45, 46 (Bd. Pat. App. & Int. 1952)). In the answer, the examiner neither repeats nor references the final rejection of claims 29 and 38 as obvious over Marshall in view of Vanderspool. (Final Rejection at 2.) Therefore, we conclude that the rejection of those claims under 35 U.S.C. § 103 has been withdrawn.

microprocessor, and clock circuitry are collocated on the same chip. A phase locked loop of the clock circuitry receives the reference clock signal and produces a sense clock signal for use by the remainder of the chip. The sense clock signal is a multiple of the reference clock signal. The test circuit counts the cycles of the sense clock signal that occur within a predetermined time, which is proportional to the reference clock's period. Alternatively, the sense clock signal and the reference clock signals may be passed through an exclusive-OR circuit and the cycles counted within a predetermined time. Either way, if the number of cycles counted is not what was expected, the sense clock signal is concluded to be incorrect.

Claim 36, which is representative for our purposes, follows:

> 36. A method for testing a clock signal generator in a data processing system, said method comprising the steps of:
>
> receiving a clock signal;
>
> receiving a reference clock signal; and
>
> determining if transition edges of said clock signal and said reference clock signal are substantially aligned by counting a number of cycles of said clock signal occurring in a predetermined period of time.

The references relied on in rejecting the claims follow:

Marshall et al. (Marshall)	4,843,617	June 27, 1989
Vanderspool, II et al. (Vanderspool)	5,398,263	Mar. 14, 1995.

Claims 27, 28, 31-33, 35-37, 40-42, and 44 stand rejected under 35 U.S.C. § 103 as obvious over Marshall in view of Vanderspool. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the totality of the record, we are persuaded that the examiner did not err in rejecting claims 27, 28, 31-33, 35-37, 40-42, and 44. Accordingly, we affirm. Our opinion addresses the grouping and obviousness of the claims.

Grouping of the Claims

When the appeal brief was filed, 37 C.F.R. § 1.192(c)(7) (1997) included the following provisions.

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and ... appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument ... why the claims are separately patentable.

Claims that are not argued separately stand or fall together.

In re Kaslow, 707 F.2d 1366, 1376, 217 USPQ 1089, 1096 (Fed. Cir. 1983). When the patentability of dependent claims is not argued separately, the claims stand or fall with the claims from which they depend. In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

Here, the appellants fail to explain why claims 27, 28, 31, 35-37, 40, and 44 are believed to be separately

patentable from each other. They also fail to explain why claims 32, 33, 41, and 42 are believed to be separately patentable from each other. Therefore, the claims stand or fall together in the following groups:

- claims 27, 28, 31, 35-37, 40, and 44.
- claims 32, 33, 41, and 42.

We select claims 36 and 42 to represent the respective groups. Next, we address the obviousness of the claims.

Obviousness of the Claims

We begin by finding that the references represent the level of ordinary skill in the art. See In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (finding that the Board of Patent Appeals and Interference did not err in concluding that the level of ordinary skill in the art was best determined by the references of record); In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("[T]he PTO usually must evaluate ... the level of ordinary skill solely on the cold words of the literature."). Of course, "'[e]very patent application and reference relies to some extent upon knowledge of persons skilled in the art to

complement that [which is] disclosed ....'" In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977) (quoting In re Wiggins, 488 F.2d 538, 543, 179 USPQ 421, 424 (CCPA 1973)). Those persons "must be presumed to know something" about the art "apart from what the references disclose." In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962). We next address the appellants' arguments regarding the obviousness of the claims.

Regarding claims 27, 28, 31-33, 35-37, 40-42, and 44, the appellants argue, "neither the *Vanderspool* patent nor the *Marshall* patent singularly or in combination teaches the limitation of determining the alignments between a clock signal and a reference clock signal by counting the number of cycles of the clock signal occurring in a predetermined period of time." (Appeal Br. at 7.)

"In the patentability context, claims are to be given their broadest reasonable interpretations. Moreover, limitations are not to be read into the claims from the

specification." In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). Here, representative claim 36 specifies in pertinent part the following limitations: "determining if ... said clock signal and said reference clock signal are substantially aligned by counting a number of cycles of said clock signal occurring in a predetermined period of time." Giving the claim its broadest reasonable interpretation, the limitations recite determining alignment between a clock signal and a reference clock signal by counting the number of cycles of the clock signal occurring in a predetermined period of time.

Marshall and Vanderspool each teach the claimed limitation. We address the references seriatim.

Marshall teaches determining alignment between a clock signal and a reference clock signal. Specifically, "a phase difference counter is utilized for detecting the phase error between a local clock signal and a received remote clock signal." Col. 1, ll. 47-50. "A correction algorithm ...

generat[es] a correction signal proportional to the detected phase error. The generated correction signal is applied to a control voltage input of the local clock oscillator for adjusting the frequency thereof ...." Id. at ll. 50-55. By detecting the phase error between the local and remote clock signals, the reference determines the alignment between the local clock signal and the remote clock signal, the latter which serves as a reference clock signal.

Marshall not only teaches determining alignment between a clock signal and a reference clock signal, but also teaches determining the alignment by counting the number of cycles of the clock signal occurring in a predetermined period of time. The reference's local clock signal is also called a "phase increment signal." Col. 2, l. 35. Marshall's phase difference counter receives the remote clock signal and the phase increment signal. Col. 7, ll. 1-2. It responsively "generat[es] a count value corresponding to the number of cycles of said phase increment signal received during each received cycle of said remote clock signal ...." Id. at ll. 2-5. By generating a count value corresponding to the number

of cycles of the phase increment signal received during each received cycle of the remote clock signal, Marshall counts a number of cycles of the phase increment signal occurring in a predetermined period of time.

Vanderspool also teaches determining alignment between a clock signal and a reference clock signal. Specifically, a "divider **725** provides a sample clock ...." Col. 7, l. 60. "[A] time-mark pulse, i.e., a one pulse-per-second (1PPS) signal, could be used to ensure that the sample rate clock is aligned to the time-mark." Id. at ll. 10-13. "A phase comparator and offset quantifier **717** receives at its inputs ... the sample clock and the 1PPS signal." Id. at ll. 62-64. The phase comparator and offset quantifier "compar[es] the time-mark signal and the sample clock signal to generate a correction signal indicating a direction of phase error. The correction signal has a duration ... for further indicating a magnitude of the phase error ...." Col. 4, ll. 9-18. By generating a correction signal indicating the phase error between the sample clock and the 1PPS signal, the reference

determines the alignment between the sample clock and the 1PPS signal, the latter which serves as a reference clock signal.

Vanderspool not only teaches determining alignment between a clock signal and a reference clock signal, but also teaches determining the alignment by counting the number of cycles of the clock signal occurring in a predetermined period of time. The reference's "phase comparator and offset quantifier **717** measures the number of incoming clock cycles difference from the rising edge of the 1PPS signal to the rising edge of the sampled clock." Col. 8, ll. 15-18. By measuring the number of incoming clock cycles difference from the rising edge of the 1PPS signal to the rising edge of the sampled clock, Vanderspool counts a number of cycles of the sampled clock occurring in a predetermined period of time.

In view of the aforementioned teachings, we are persuaded that either Marshall or Vanderspool, in combination with the prior art as a whole, teaches the claimed limitation of "determining if ... said clock signal and said reference clock

signal are substantially aligned by counting a number of cycles of said clock signal occurring in a predetermined period of time." Therefore, we affirm the rejection of claims 27, 28, 31, 35-37, 40, and 44 as obvious over Marshall in view of Vanderspool.

Further regarding claims 32, 33, 41, and 42, the appellants argue, "neither *Marshall* nor *Vanderspool* teaches that the number of cycles counted within the determining circuitry or step is equal to the multiple when the clock signal generator is operating correctly." (Appeal Br. at 8.)

Representative claim 41 specifies in pertinent part the following limitations: "said clock signal ... is equal to a multiple of said reference clock signal" and "said number of cycles is equal to said multiple when said clock signal generator is operating correctly." Giving the claim its broadest reasonable interpretation, the limitations recite that the frequency of the clock signal is a multiple of the frequency of the reference clock signal and that the number of cycles of the clock signal occurring in a predetermined period

of time is equal to the multiple when the clock signal generator is operating correctly.

Both Marshall and Vanderspool teach the claimed limitations. We address the references seriatim.

Marshall teaches that the frequency of the clock signal is a multiple of the frequency of the reference clock signal. Specifically, the reference's local clock signal "is an approximately 512 kilohertz phase increment signal." Col. 2, ll. 35-56. Marshall's remote clock signal, which serves as a reference clock signal, has a frequency of 4 kHz. Col. 3, ll. 10-12. The phase increment signal's frequency of 512 kHz is 128-times greater than the remote clock signal's frequency of 4 kHz. By employing a phase increment signal frequency that is 128-times greater than the remote clock signal frequency, the reference teaches that the frequency of the clock signal is a multiple of the frequency of the reference clock signal.

Marshall further teaches that the number of cycles of the clock signal occurring in a predetermined period of time is equal to the multiple when the clock signal generator is operating correctly. As aforementioned regarding the appellants' first argument, the reference counts a number of cycles of the phase increment signal occurring during each cycle of the remote clock signal. Because the frequency of the phase increment signal is 128-times greater than that of the remote clock signal, 128 cycles would be counted when the apparatus of the Marshall is operating properly.

Vanderspool also teaches that the frequency of the clock signal is a multiple of the frequency of the reference clock signal. Specifically, the reference's sample clock has a frequency of 50 kHz. Col. 8, ll. 3-4. Vanderspool's 1PPS signal, which serves as a reference clock signal, has a frequency of "one pulse-per-second," col. 7, l. 11, or 1 Hz. The sample clock's frequency of 50 kHz is 50,000-times greater than the 1PPS signal's frequency of 1 Hz. By employing a sample clock frequency that is 50,000-times greater than the 1PPS signal's frequency, the reference teaches that the

frequency of the clock signal is a multiple of the frequency of the reference clock signal.

Vanderspool further teaches that the number of cycles of the clock signal occurring in a predetermined period of time is equal to the multiple when the clock signal generator is operating correctly. As aforementioned regarding the appellants' first argument, the reference counts a number of cycles of the sampled clock occurring during each cycle of the 1PPS signal. Because the frequency of the sampled clock is 50,000 times greater than that of the 1PPS signal, 50,000 cycles would be counted when the apparatus of the Vanderspool is operating properly.

In view of the aforementioned teachings, we are persuaded that either Marshall or Vanderspool, in combination with the prior art as a whole, teaches the claimed limitation of "said clock signal ... is equal to a multiple of said reference clock signal" and "said number of cycles is equal to said multiple when said clock signal generator is operating correctly." Therefore, we affirm the rejection of claims 32,

33, 41, and 42 as obvious over Marshall in view of Vanderspool.

We end by noting that our affirmance is based only on the arguments made in the briefs. Arguments not made therein are not before us, are not at issue, and are considered waived.

CONCLUSION

To summarize, the rejections of claims 27, 28, 31-33, 35-37, 40-42, and 44 under 35 U.S.C. § 103 as obvious over Marshall in view of Vanderspool is affirmed.

No period for taking subsequent action concerning this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

JAMES D. THOMAS Administrative Patent Judge	)
JERRY SMITH Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)

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